UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,124	12/31/2001	Theodore W. Houston	TI-32107 (032350.B369)	1057

23494 7590 12/18/2002

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/039,124	Applicant(s) HOUSTON ET AL.
	Examiner Johannes P Mondt	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

The examiner has considered the item listed in the Information Disclosure Statement of Paper No. 2.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 1-2, 4-6, 9, 13-14, 20-21, 23-27, 31-32 and 34-35*** are rejected under 35 U.S.C. 102(b) as being anticipated by Forbes et al (6,104,061).

With regard to claims 1 and 20: Referring to Figures 8-11; column 12, line 27-column 13, line 15 and column 13, line 52-67), Forbes et al teach a memory array (cf. column 2, lines 28-29) comprising:

a bit cell row comprising a bit cell (cf. column 4, lines 43-67), the bit cell (trench 121 and surroundings) comprising a first transistor 130 disposed in a bit cell body region (that portion of 214 that surrounds trench 221 (cf. column 7, lines 31-33)), the first transistor including a first active region (in said body region along gate oxide 218);

a strap cell row comprising a strap cell (cf. column 12, lines 34-39), the strap cell (trench 122 and surroundings) comprising a first strap cell body region conductively coupled to the first bit cell body region (cf. column 12, lines 37-39);

a first power supply line electrically coupled to the first active region and providing a first supply voltage to the first active region (world line, coupled to the active region of the FET, the word line WL (cf. Figure 1 and column 4, lines 53-67) governing the gate voltage and thus determining the channel conductivity, the channel residing in the active region of the FET by setting the voltage across the channel); and

a first offset supply line R1, R2, etc., (cf. Figure 1 and column 4, lines 63-67) electrically coupled to the first strap cell body region and providing a first offset voltage to the first bit cell body region via the first strap cell body region (cf. column 12, lines 34-43), wherein the first supply voltage is operable to be different from the first offset voltage (cf. column 12, lines 44-64).

In conclusion, Forbes et al anticipate claim 1. Because Forbes et al specifically teach the memory device to be designed to reduce leakage currents Forbes et al also anticipate claim 20.

With regard to claims 2 and 21: the first supply voltage potential as taught by Forbes et al is operable to be different from the first offset voltage in a standby mode of the bit cell (cf. column 7, lines 1-18). Because Forbes et al specifically teach the memory device to be designed to reduce leakage currents Forbes et al also anticipate claim 21.

With regard to claims 4, 23 and 24: the difference between the first offset voltage and the first supply voltage as taught by Forbes et al is operable to be controlled such that the said difference is greater in a standby mode of the bit cell (namely: 1.5 Volt) than in an active mode of the bit cell (approximately 1 Volt) (cf. column 7, lines 1-18).

Because Forbes et al specifically teach the memory device to be designed to reduce leakage currents Forbes et al also anticipate claims 23 and 24.

With regard to claim 5 and 25: the first transistor 130 as taught by Forbes et al is an n-channel transistor (cf. column 5, lines 45-59), wherein the first bit cell body is a p-type substrate (cf. column 5, lines 50-52), wherein the first offset voltage is a substrate voltage, wherein the first supply voltage is a low power supply voltage (inherently, by virtue of being a word line voltage), and wherein the first supply voltage is operable to be greater than the first offset voltage (cf. column 7, lines 1-18). Because Forbes et al specifically teach the memory device to be designed to reduce leakage currents Forbes et al also anticipate claim 25.

With regard to claim 6 and 26: the memory array as taught by Forbes et al (cf. Figure 1) is coupled to a peripheral circuit 116 (cf. column 5, lines 8-16), wherein the peripheral circuit has a low power supply voltage, and wherein the first supply voltage of the memory array is operable to be greater than the low power supply voltage of the peripheral circuit (cf. column 7, lines 1-18). Because Forbes et al specifically teach the memory device to be designed to reduce leakage currents Forbes et al also anticipate claim 26.

With regard to claim 9 and 27: the bit cell as taught by Forbes et al comprises a bit cell geometry and the strap cell comprises a strap cell geometry substantially similar to the bit cell geometry (cf. Figure 10, for side-by-side comparison of the bit and strap cell geometries; for instance trenches for bit cell and strap cell, and corresponding word line and body contact regions 206 and 208, respectively). Because Forbes et al

specifically teach the memory device to be designed to reduce leakage currents Forbes et al also anticipate claim 27.

With regard to claim 13: the memory array of claim 1 as taught by Forbes et al comprises a conductive layer (206a within the trench dug within 216 in Figure 10 or Figure 11D) and a word line (cf. column 7, line 45) formed in said conductive layer and electrically coupled to the bit cell (said word line forming the gate in this manner), and wherein the first offset supply line is formed in the conductive layer.

With regard to claim 14: the first supply voltage as taught by Forbes et al may be controlled separately from the first offset voltage (cf. column 7, lines 1-18).

With regard to claim 31: the first strap cell body region (region within 214 abutting 208a in Figure 10) as taught by Forbes et al is operable to be coupled to a first bit cell body region (region within 214 contiguous with the active region abutting gate oxide 218 to the right of 206b in Figure 10) of a bit cell comprising a first transistor including a first active region disposed in the first bit cell body region (cf. column 12, lines 27-64); wherein the strap cell is operable to communicate a first offset voltage from a first offset supply line (208a is connected to offset supply line R; see column 4, lines 53-67) to the first bit cell body region via the first conductive contact 208a and the aforementioned first strap cell body region; and wherein the first offset voltage is operable to be different from a first supply voltage received by the first active region from a first power supply line (cf. column 7, lines 1-18).

With regard to claim 32: the first supply voltage potential as taught by Forbes et al is operable to be different from the first offset voltage in a standby mode of the bit cell (cf. column 7, lines 1-18).

With regard to claim 34: the difference between the first offset voltage and the first supply voltage as taught by Forbes et al is operable to be controlled such that the said difference is greater in a standby mode of the bit cell (namely: 1.5 Volt) than in an active mode of the bit cell (approximately 1 Volt) (cf. column 7, lines 1-18).

With regard to claim 35: the bit cell as taught by Forbes et al comprises a bit cell geometry and the strap cell comprises a strap cell geometry substantially similar to the bit cell geometry (cf. Figure 10, for side-by-side comparison of the bit and strap cell geometries; for instance trenches for bit cell and strap cell, and corresponding word line and body contact regions 206 and 208, respectively).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. ***Claims 3, 7-8, 22, 33 and 37*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes et al (6,104,061).

With regard to claims 3 and 22, Forbes et al anticipate claim 1 (see above). Forbes do teach that during an active mode of the bit cell the difference between the

first supply voltage of the word line and the first offset voltage as applied to the body contact line is substantially reduced by 33% to about 1 Volt (from 1.5 Volt during standby) for the specific purpose of decrease the magnitude of the turn-on threshold voltage ands thus to increase the effective gate overdrive voltage provided on the word line. The range of this reduction is different from the one expressed in claim 3, which claim calls for a reduction by 100% to 0 Volt of said difference. However, Applicant's disclosure fails to show that such a further reduction would be critical to the invention. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. Because Forbes et al specifically teach the memory device to be designed to reduce leakage currents claim 22 is also unpatentable over the same prior art.

With regard to claim 7-8: Forbes et al do not necessarily teach the further limitations of claims 7-8; however, said further limitations only differ by full interchange of n-type and p-type conductivities and corresponding voltages from the further limitations of claims 5-6. It is understood as obvious in the art of semiconductor device technology that such interchange generally is not patentable when the general conditions of the claim are met without such interchange, as is the case here (see claims 5-6 as rejected above under U.S.C. 102(b)).

With regard to claim 33: Forbes et al anticipate claim 32, as discussed above. Forbes do teach that during an active mode of the bit cell the difference between the first supply voltage of the word line and the first offset voltage as applied to the body

contact line is substantially reduced by 33% to about 1 Volt (from 1.5 Volt during standby) for the specific purpose of decrease the magnitude of the turn-on threshold voltage ands thus to increase the effective gate overdrive voltage provided on the word line. The range of this reduction is different from the one expressed in claim 33, which claim calls for a reduction by 100% to 0 Volt of said difference. However, Applicant's disclosure fails to show that such a further reduction would be critical to the invention. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With regard to claim 37: the strap cell in claim 31 as anticipated by Forbes et al is a member of a logical circuit (116; cf. Figure 1), wherein the logical circuit inherently has a logic circuit supply voltage regulated by the same logical circuit as the first supply voltage (WL or word line). Forbes et al do not necessarily teach the further limitation of claim 37. Forbes do teach that during an active mode of the bit cell the difference between the first supply voltage of the word line and the first offset voltage as applied to the body contact line is substantially reduced by 33% to about 1 Volt (from 1.5 Volt during standby) for the specific purpose of decrease the magnitude of the turn-on threshold voltage ands thus to increase the effective gate overdrive voltage provided on the word line. The range of this reduction is different from the one expressed in claim 37, which claim calls for a reduction by 100% to 0 Volt of said difference, because this is the significance of the requirement that the first supply voltage be the same as the logic circuit supply voltage. However, Applicant's disclosure fails to show that having the

same voltage in this regard would be critical to the invention. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

5. ***Claims 10-12, 28 and 36*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes et al (6,104,061) in view of Wolf (ISBN 0-961672-4-5). As detailed above, Forbes et al anticipate claim 1. Forbes et al do not necessarily teach the further limitation as defined by claims 10, 11, 12, 28, or 36. However, in an effort to reduce leakage current it would have been obvious to one of ordinary skills to select CMOSFETs for the memory bit cells, because it has long been known in the art of semiconductor memory devices that CMOS technology allows the suppression of current dissipation during standby operation (see Wolf, pages 368-373, particularly page 370, first paragraph). Inherent in the change from the device of claim 1 to the CMOSFET is the addition of a second transistor to the bit cell disposed in an n-well region extending generally along a first direction, namely: the direction parallel to the upper main surface of the substrate, which also is the direction of said bit line as the latter has to connect with adjacent transistor cell drain regions (*claim 10*); while with a flip-flop configuration such as offered by CMOSFET bit cells the memory is retained as long as the power is on, while the latter is affordable through the sharply reduced leakage current (see Wolf, pages 572-576, especially the first paragraph of section 8.2) (*claim 11*); and while the typical CMOS SRAM unit consists, when efficiently built, of six

transistors (cf. Figure 8-2(b) in Wolf on page 573) (*claim 12*). Because Forbes et al specifically teach the memory device to be designed to reduce leakage currents claim 28 is also unpatentable over the same prior art.

With regard to claim 36: As detailed above, Forbes et al anticipate claim 31. Forbes et al do not necessarily teach the further limitation as defined by claim 36. However, in an effort to reduce leakage current it would have been obvious to one of ordinary skills to select CMOSFETs for the memory bit cells, because it has long been known in the art of semiconductor memory devices that CMOS technology allows the suppression of current dissipation during standby operation (see Wolf, pages 368-373, particularly page 370, first paragraph). Inherent in the change from the device of claim 31 to the CMOSFET is the addition of a second transistor to the bit cell disposed in an n-well region extending generally along a first direction, namely: the direction parallel to the upper main surface of the substrate, which also is the direction of said bit line as the latter has to connect with adjacent transistor cell drain regions.

6. ***Claims 15-17, 29-30 and 38-39*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes et al (6,104,061) in view of Wolf (ISBN: 0-961672-4-5) and Keshavarzi et al (ISBN: 1-58113-133-X). As detailed above, Forbes et al anticipates claim 1 while a CMOS implementation of Forbes' invention is obvious over Wolf (see rejection of claims 10-12 under 103(a) as given above). Forbes et al nor Wolf necessarily teach the further limitation of claim 15. However, as shown by Keshavarzi et al, current leakage during standby in CMOS integrated circuits, hence also inherently in

a CMOS memory array would be minimized by applying reverse body bias not just to the substrate but also to the well (see abstract and first sentence of section 2 on page 252). Therefore, it would have been obvious to one of ordinary skills to include, in the CMOS invention as essentially taught by Forbes et al in view of Wolf, separate body contacts to both the semiconductor substrate (for the n-channel transistor) and the n-well (for the p-channel transistor). When the teaching in this regard by Keshavarzi et al is implemented said CMOS memory array is characterized such that the bit cell further comprises a second (p-channel) transistor disposed in a second bit cell body region (namely the n-well), the second transistor including a second active region (the p channel), wherein the strap cell further comprises a second strap cell body region conductively coupled to the second bit cell body region; and wherein the memory array further comprises: a second power supply line electrically coupled to the second active region (word line for the gate of the p-channel transistor) and providing a second supply voltage to the second active region (gate voltage); and a second offset supply line electrically coupled to the second strap cell body region and providing a second offset voltage to the second bit cell body region, wherein in full analogy with the different operability of first supply and first offset voltages, the second supply voltage is operable to be different than the second offset voltage.

Motivation for the inclusion of the teaching by Keshavarzi et al in this regard is the objective by Forbes et al to minimize leakage current (see "Background of Invention" in Forbes et al, particularly lines 39-52 of column 1). *Combinability* of said teaching with said invention is ensured because the standard adaptation in a sub-combination

(namely the standard implementation of separate body contacts for the two transistors in a CMOSFET) does not impact on the array design other than the need for an additional body contact line, such as provided for the R1, R2, etc., in Forbes et al. *Success* in the implementation of said combination can therefore be reasonably expected.

Because Forbes et al specifically teach the memory device to be designed to reduce leakage currents claim 29 is also unpatentable over the same prior art.

With regard to claims 16 and 30: the further limitation of claim 15 would be disclosed by the prior art as cited for claim 5 through an overall interchange of n- and p-type conductivities. It is understood in the semiconductor technology art that when the general conditions are met by the prior art an overall interchange of all conductivity types does not distinguish over the same prior art either, unless Applicant can show that aforementioned overall interchange is critical to the invention. No such evidence is evident from Applicant's disclosure. Because Forbes et al specifically teach the memory device to be designed to reduce leakage currents claim 30 is also unpatentable over the same prior art.

With regard to claim 17: with reference to the discussion of claim 6 and claim 15 as given above, Forbes et al in view of Wolf and Keshavarzi et al teach the memory array of claim 15 to be coupled to a peripheral circuit. By necessity the separate body contacts for the substrate and the well when aiming to reduce leakage current must ameliorate gate voltages of opposite polarity and hence require the said low power supply voltage and the high power supply voltage as expressed by claim 17, while the

substantial equality (or sameness) of the first offset voltage and the high power supply voltage of the peripheral circuit and the substantial equality of the second offset voltage and the low power supply voltage of the peripheral circuit are in evidence from the circuit shown in Figure 1 of Forbes et al, wherein no substantial resistance or impedance is shown between said peripheral circuit 116 and the body contact provided by R1, R2, etc..

With regard to claim 38: Forbes et al nor Wolf necessarily teach the further limitation of claim 38. However, as shown by Keshavarzi et al, current leakage during standby in CMOS integrated circuits, hence also inherently in a CMOS memory array would be minimized by applying reverse body bias not just to the substrate but also to the well (see abstract and first sentence of section 2 on page 252). Therefore, it would have been obvious to one of ordinary skills to include, in the CMOS invention as essentially taught by Forbes et al in view of Wolf, separate body contacts to both the semiconductor substrate (for the n-channel transistor) and the n-well (for the p-channel transistor). With reference to the discussion of claim 15: when the teaching in this regard by Keshavarzi et al is implemented said CMOS memory array is inherently characterized to include a second strap cell body region operable to be conductively coupled to the second bit cell body region; and wherein a second transistor including a second active region is disposed in the second bit cell body; and a second conductive contact coupled to the second strap body region; wherein the strap cell is operable to communicate a second offset voltage from a second offset supply line to the second bit cell body region via the second conductive contact and the second strap cell body

region; and wherein in full analogy with the different operability of first supply and first offset voltages, the second offset voltage is operable to be different from a second supply voltage received from a second power supply line.

With regard to claim 39: the first transistor 130 as taught by Forbes et al is an n-channel transistor (cf. column 5, lines 45-59), wherein the first bit cell body is a p-type substrate (cf. column 5, lines 50-52), wherein the first offset voltage is a substrate voltage, wherein the first supply voltage is a low power supply voltage (inherently, by virtue of being a word line voltage), and wherein the first supply voltage is operable to be greater than the first offset voltage (cf. column 7, lines 1-18). Therefore, the further limitation of claim 38 would be disclosed by the prior art as cited for the device of claim 38 through an overall interchange of n- and p- type conductivities. It is understood in the semiconductor technology art that when the general conditions are met by the prior art an overall interchange of all conductivity types does not distinguish over the same prior art either, unless Applicant can show that aforementioned overall interchange is critical to the invention. No such evidence is evident from Applicant's disclosure.

7. ***Claims 18-19*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes et al, Wolf and Keshavarzi et al as applied to claim 15 above, and further in view of De et al (6,218,895). It is understood in the art of transistor body contact technology that body contacts are provided through conductive layers so as to smoothen the transition in the electric resistivity from (lowly doped) semiconductor to metallic conductor. In the present device as essentially taught by Forbes et al in view of Wolf

and Keshavarzi et al there are two body contacts needed, one to the substrate, and one to the well in the substrate; hence, in addition to the bit cell to which the bit line is coupled (as discussed before, this aspect is taught by Forbes et al) it would have been obvious to one of ordinary skills to provide a first conductive layer and a second conductive layer wherein the first and second offset supply lines are formed. De et al provide the specific teaching in this respect (cf. front figure and abstract).

Motivation to incorporate the teaching in this respect by De et al is the avoidance of sharp transitions in the conductivity involved in the body contact. Combinability is straightforward because the implementation of body contacts through conductive layers is standard in the art as shown by De et al. Success in implementing the combination can therefore be reasonably expected.

With regard to claim 19: the memory array of claim 18 as essentially taught by Forbes et al, Wolf, Keshavarzi et al and De et al has the bitline connect to the source and drain conductive layer, as evidenced by De et al, Figure 4; thus the memory array further comprises a third conductive layer (source and drain) 216 (cf. column 9, line 52 in Forbes et al) and a bit line electrically coupled to the bit cell, wherein the first power supply line, the second power supply line, and the bit line are formed in the third conductive layer (cf. Fig. 14 and front figure in De et al). Therefore, claim 19 does not distinguish over the prior art.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hidaka et al (6,018,895).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
December 12, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800